



On-Line Class



Wireline SERDES Transceivers

JULY 13-17, 2020

PST - California Time Zone

Monday, July 13

08:00 - 09:30 am	Introduction to Wireline Transceivers	Pavan Hanumolu
10:00 - 11:30 am	Transmitters (CML/VM)	Pavan Hanumolu
01:00 - 02:30 pm	FIR Equalizers (Tx/Rx)	Pavan Hanumolu
03:00 - 04:30 pm	Receivers (CTLE, DFE, Adaptation)	Pavan Hanumolu

Tuesday, July 14

08:00 - 09:30 am	Phase-Locked Loops	Pavan Hanumolu
10:00 - 11:30 am	Phase-Locked Loops	Pavan Hanumolu
01:00 - 02:30 pm	Advanced PLLs	Pavan Hanumolu
03:00 - 04:30 pm	Clock and Data Recovery	Pavan Hanumolu

Wednesday, July 15

08:00 - 09:30 am	Advance Signaling Methods	Armin Tajalli
10:00 - 11:30 am	Short Reach Transceiver Design Tradeoffs	Armin Tajalli
01:00 - 02:30 pm	Tradeoffs in Design of Slicers	Armin Tajalli
03:00 - 04:30 pm	Discrete-Time Front-End Design	Armin Tajalli

Thursday, July 16

08:00 - 09:30 am	Clock and Data Recovery (ct'd)	Pavan Hanumolu
10:00 - 11:30 am	Baud-Rate CDRs	Pavan Hanumolu
01:00 - 02:30 pm	Introduction to PAM4 Signaling	Pavan Hanumolu
03:00 - 04:30 pm	Trans-impedance amplifiers	Pavan Hanumolu

Friday, July 17

08:00 - 09:30 am	Optical Transmitters	Sam Palermo
10:00 - 11:30 am	Design of ADC-Based Serial Links	Sam Palermo

